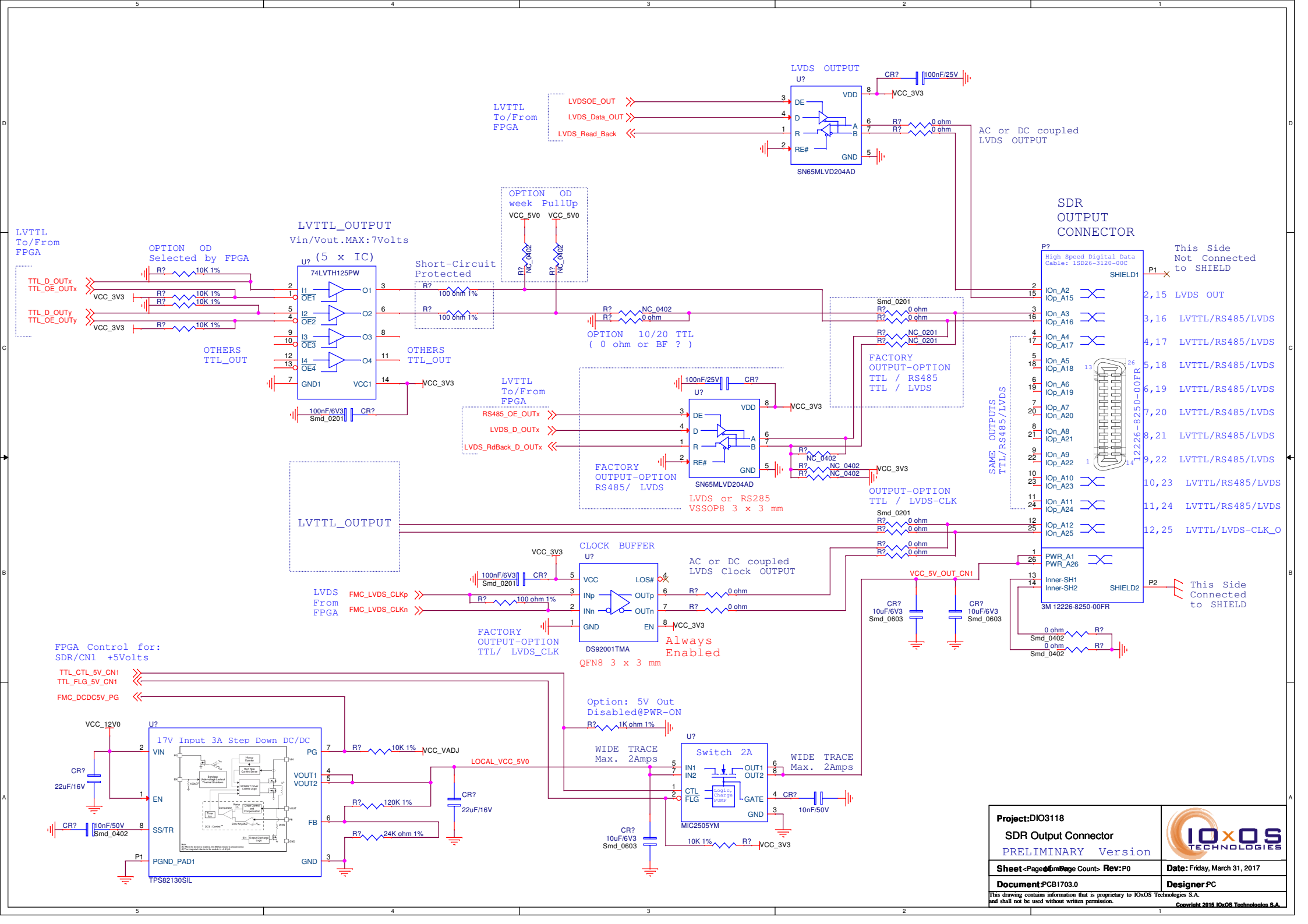
LVTTL To/From FPGA
LVDS OUTPUT
LVDSOE_OUT
LVDS_Data_OUT
LVDS_Read_Back
SN65MLVD204AD
AC or DC coupled LVDS OUTPUT
SDR OUTPUT CONNECTOR
LVTTL_OUTPUT
Vin/Vout.MAX:7Volts
(5 x IC)
74LVTH125PW
OPTION OD Selected by FPGA
OPTION OD week PullUp
Short-Circuit Protected
OPTION 10/20 TTL ( 0 ohm or BF ? )
OTHERS TTL_OUT
FACTORY OUTPUT-OPTION TTL / RS485 TTL / LVDS
SAME OUTPUTS TTL/RS485/LVDS
RS485_OE_OUTx
LVDS_D_OUTx
LVDS_RdBack_D_OUTx
FACTORY OUTPUT-OPTION RS485/ LVDS
LVDS or RS285 VSSOP8 3 x 3 mm
OUTPUT-OPTION TTL / LVDS-CLK
LVTTL_OUTPUT
CLOCK BUFFER
LVDS From FPGA
FMC_LVDS_CLKp
FMC_LVDS_CLKn
AC or DC coupled LVDS Clock OUTPUT
DS92001TMA
FACTORY OUTPUT-OPTION TTL/ LVDS_CLK
Always Enabled
QFN8 3 x 3 mm
FPGA Control for: SDR/CN1 +5Volts
TTL_CTL_5V_CN1
TTL_FLG_5V_CN1
FMC_DCDC5V_PG
17V Input 3A Step Down DC/DC
TPS82130SIL
Option: 5V Out Disabled@PWR-ON
WIDE TRACE Max. 2Amps
Switch 2A
MIC2505YM
LOCAL_VCC_5V0
VCC_VADJ
VCC_5V_OUT_CN1
High Speed Digital Data Cable: 1SD26-3120-00C
3M 12226-8250-00FR
This Side Not Connected to SHIELD
This Side Connected to SHIELD
2,15 LVDS OUT
3,16 LVTTL/RS485/LVDS
4,17 LVTTL/RS485/LVDS
5,18 LVTTL/RS485/LVDS
6,19 LVTTL/RS485/LVDS
7,20 LVTTL/RS485/LVDS
8,21 LVTTL/RS485/LVDS
9,22 LVTTL/RS485/LVDS
10,23 LVTTL/RS485/LVDS
11,24 LVTTL/RS485/LVDS
12,25 LVTTL/LVDS-CLK_O
Project:DIO3118
SDR Output Connector
PRELIMINARY Version
Sheet <Page Number> of <Page Count> Rev:P0
Date: Friday, March 31, 2017
Document:PCB1703.0
Designer:PC
This drawing contains information that is proprietary to IOxOS Technologies S.A. and shall not be used without written permission.
Copyright 2015 IOxOS Technologies S.A.